IN THE CLAIMS

Please amend the claims as follows:

1-6. (Canceled)

7. (Currently Amended) A processor comprising:

a processor core including a general-purpose register, an instruction decoder, and a second execution unit;

an extension unit including a first execution unit connected to the processor core; and

a direct memory access controller connected to both the processor core and the extension unit;

~~The processor of claim 2,~~ wherein the first execution unit is a reconfigurable first execution unit.

8. (Original) The processor of claim 7, wherein the extension unit further comprises an instruction decoder, a control register, and local memory.

9. (Original) The processor of claim 7, wherein the instruction decoder in the extension unit further comprises a reconfigurable logic circuit that is the same as the reconfigurable first execution unit.

10. (Original) The processor of claim 7, wherein configuration data provided to the reconfigurable logic circuit, is provided through data transmission from the direct access memory controller via a configuration interface connecting the reconfigurable first execution unit in the extension unit and the direct memory access controller.

11. (Previously Presented) The processor of claim 8, wherein configuration data provided to the reconfigurable logic circuit is stored in the local memory of the extension unit.

12-16. (Canceled)

17. (Currently Amended) A semiconductor integrated circuit, comprising:

a semiconductor chip;

a processor core integrated on the semiconductor chip including a general purpose register, an instruction decoder, and a second execution unit;

an extension unit integrated on the semiconductor chip including a first execution unit connected to the processor core;

a direct memory access controller integrated on the semiconductor chip and connected to both the processor core and the extension unit;

~~The semiconductor integrated circuit of claim 13,~~ wherein the first execution unit is a reconfigurable first execution unit.

18. (Original) The semiconductor integrated circuit of claim 17, wherein the instruction decoder in the extension unit further comprises a reconfigurable logic circuit that is the same as the reconfigurable first execution unit.

19. (Previously Presented) The semiconductor integrated circuit of claim 18, wherein configuration data provided to the reconfigurable logic circuit, is provided through data transmission from the direct access memory controller via a configuration interface

connecting between the reconfigurable first execution unit in the extension unit and the direct memory access controller.

20. (Previously Presented) The semiconductor integrated circuit of claim 18, wherein configuration data provided to the reconfigurable logic circuit is stored in internal local memory of the extension unit.